SUB C5

13. (amended) The method of claim 12, further comprising forming sidewall spacers along the sides of gate stack structures, wherein said etching is performed such that the sidewall spacers of said gate stack structures are not etched, wherein said sidewall spacers define at least in part said opening formed in said insulative layer.

B2

14. (amended) The method of claim 1, further comprising forming sidewall spacers along the sides of gate stack structures, wherein said etching is performed such that the sidewall spacers of said gate stack structures are not etched, wherein said sidewall spacers define at least in part said opening formed in said insulative layer.

SUB C9

36. (twice amended) A process for forming an opening in an insulative layer formed over a substrate in a semiconductor device, comprising:

B3

forming a pair of adjacent gate stacks in said insulative layer;

forming sidewall spacers on sidewalls of said adjacent gate stacks;

forming a patterned photoresist mask layer over said insulative layer; and,

etching an opening in said insulative layer through an aperture in said patterned resist layer, wherein said opening is etched through to said substrate using a combination of ammonia and at least one fluorocarbon, wherein said fluorocarbon is selected from the group consisting of C_4F_8, C_4F_6, C_5F_8, CF_4, C_2F_6, and C_3F_8, and wherein the flow rate ratio of said at least one fluorocarbon to said ammonia is from about 2:1 to about 40:1.

B4

43. (twice amended) The process of claim 42, wherein said opening is formed between said sidewall spacers on said pair of adjacent gate stacks.

SUB C13

B5

64. (twice amended) A method of forming a conductive plug between adjacent gate stacks with sidewall spacers and inside a self-aligned contact opening formed in an insulative layer provided over a substrate in a semiconductor device, comprising:

SUB C13

contacting said insulative layer with a plasma etchant mixture consisting essentially of ammonia and at least one fluorocarbon at a temperature within the range of from about -50 to about 80 degrees Celsius so as to form a self-aligned contact opening defined at least in part by said sidewall spacers on adjacent gate stacks in said insulative layer without an etch stop, wherein said contacting further forms a protective layer over opposed sidewall spacers which have been formed over said adjacent gate stacks, wherein the flow rate ratio of said at least one flurocarbon to said ammonia is from about 2:1 to about 40:1; and,

depositing a conductive plug inside said etched opening such that said conductive plug is separated from said sidewall spacers by said protective layer.